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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

MILORD, MARCEAU

ART UNIT	PAPER NUMBER
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2682

23

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/698,497

Applicant(s)

ROFOUGARAN ET AL.

Examiner

Marceau Milord

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 April 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hilbert (US Patent No 5983082) in view of Gardenfors et al (US Patent No 6633550 B1)

Regarding claim 1, Hilbert discloses a circuit (fig. 8), comprising: a logic circuit (420 of fig. 8); a capacitor (805 or 806 of fig. 8; col. 11, line 21- col. 12, line 13); a first resistor (814 of fig. 8) having a first end coupled to the power input and a second end to couple to a power source (col. 12, lines 26 -32); and a second resistor (815 of fig. 8; col. 12, line 33- col. 13, line 65; col. 14, lines 11- 65).

However, Hilbert does not specifically disclose a capacitor coupled across the power input and the power return; and a first resistor having a first end coupled to the power input and a second end to couple to a power source.

On the other hand, Gardenfors et al, from the same field of endeavor, discloses a radio transceiver that can be completely integrated into one IC chip. A single, directly modulated VCO is used for both up-conversion during transmission, and down-conversion during reception. Furthermore, Gardenfors shows in figure 5, a transceiver on a chip, which includes a transmit/receive antenna coupled to a low noise amplifier in the receiver front end. The output of the low noise amplifier is coupled to an image-rejection mixer, which is also composed of a first

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mixer 206 for the I channel, a second mixer 208 for the Q channel, several phase shifters, and combiner (figs. 3-4; col. 5, line 41- col. 6, line 47). The transceiver on a chip also includes a phase locked loop, which is composed of a phase detector, a loop filter, and a prescaler with modulus logic 240. The phase locked loop is a component of a synthesizer, a charge pump, and a modulus logic circuitry 238 (fig. 5; col. 6, lines 48-67; col. 7, lines 1-44). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Gardenfors to the system of Hilbert in order to produce a short-range radio transceiver on a single integrated circuit chip.

Regarding claims 2- 5, Hilbert as modified discloses a circuit (fig. 8), comprising: a logic circuit (420 of fig. 8) wherein the logic circuit comprises a differential circuit; wherein the two logic gates each comprises an inverter (col. 11, lines 21-66).

Regarding claims 7 and 16, Hilbert as modified discloses a circuit (fig. 8), comprising: a logic circuit (420 of fig. 8) wherein the CMOS inverters each comprises a p-channel transistor having a source coupled to the power input, a gate, and a drain, and an n-channel transistor having a source coupled to the power return, a gate coupled to the gate of the p-channel transistor to form an input node, and a drain coupled to the drain of the p-channel transistor to form output node (col. 11, line 21- col. 12, line 32), the differential circuit further having a differential input comprising the input nodes for each of the CMOS inverters, and a differential output comprising the output nodes for each of the CMOS inverters (col. 13, line Scot. 14, line 60).

Regarding claim 8, Hilbert discloses a circuit (fig. 8), comprising: logic means (809 of fig. 8) for performing a logic function (col. 11, line 21- col. 12, line 13); charge means (805 or

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806 of fig. 8) for storing a charge across the logic means (fig. 8; col. 12, line 33- col. 13, line 65; col. 14, lines 11- 65).

However, Hilbert does not specifically disclose an isolation means for isolating the charge means from a power source.

On the other hand, Gardenfors et al, from the same field of endeavor, discloses a radio transceiver that can be completely integrated into one IC chip. A single, directly modulated VCO is used for both up-conversion during transmission, and down-conversion during reception. Furthermore, Gardenfors shows in figure 5, a transceiver on a chip, which includes a transmit/receive antenna coupled to a low noise amplifier in the receiver front end. The output of the low noise amplifier is coupled to an image-rejection mixer, which is also composed of a first mixer 206 for the I channel, a second mixer 208 for the Q channel, several phase shifters, and combiner (figs. 3-4; col. 5, line 41- col. 6, line 47). The transceiver on a chip also includes a phase locked loop, which is composed of a phase detector, a loop filter, and a prescaler with modulus logic 240. The phase locked loop is a component of a synthesizer, a charge pump, and a modulus logic circuitry 238 (fig. 5; col. 6, lines 48-67; col. 7, lines 1-44). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Gardenfors to the system of Hilbert in order to produce a short-range radio transceiver on a single integrated circuit chip.

Regarding claims 9-10, Hilbert as modified discloses a circuit (fig. 8), comprising: a logic circuit (420 of fig. 8) wherein the charge means comprises a capacitor (805 or 806 of fig. 8); and the isolation means comprises a first resistor (814 of fig. 8) to couple a first end of the capacitor to the power source (col. 12, lines 26 32), a second resistor (815 of fig. 8) to couple a second end

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of the capacitor to a return line for the power source (col. 12, line 33- col. 13, line 65; col. 14, lines 11- 65).

Claims 11-15 contain similar limitations addressed in claims 2-7, and therefore are rejected under a similar rationale.

Regarding claims 17-18, Hilbert discloses a method (fig. 3 and fig. 8) of suppressing noise during the switching of a differential circuit having differential inputs and outputs, comprising: charging a capacitor (805 or 806 of fig. 8) through a resistor (814 of fig. 8; col. 11, line 21- col. 12, line 13); applying a signal transition at the differential inputs (col. 9, line 22col. 10, line 66); and circulating charge between the differential outputs (col. 12, lines 26 -32); compensating for loss of the charge on the capacitor during the circulation of charge (col. 12, line 33- col. 13, line 65 ; col. 14, lines 11- 65).

However, Hilbert does not specifically disclose the features of circulating charge between the differential outputs through the capacitor; compensating for loss of the charge on the capacitor during the circulation of charge by recharging the capacitor through the resistor.

On the other hand, Gardenfors et al, from the same-field of endeavor, discloses a radio transceiver that can be completely integrated into one IC chip. A single, directly modulated VCO is used for both up-conversion during transmission, and down-conversion during reception. Furthermore, Gardenfors shows in figure 5, a transceiver on a chip, which includes a transmit/receive antenna coupled to a low noise amplifier in the receiver front end. The output of the low noise amplifier is coupled to an image-rejection mixer, which is also composed of a first mixer 206 for the I channel, a second mixer 208 for the Q channel, several phase shifters, and combiner (figs. 3-4;col. 5, line 41- col. 6, line 47). The transceiver on a chip also includes a

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phase locked loop, which is composed of a phase detector, a loop filter, and a prescaler with modulus logic 240. The phase locked loop is a component of a synthesizer, a charge pump, and a modulus logic circuitry 238 (fig. 5; col. 6, lines 48-67; col. 7, lines 1-44). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Gardenfors to the system of Hilbert in order to produce a short-range radio transceiver on a single integrated circuit chip.

Regarding claim 19, Hilbert as modified discloses a method (fig. 8) of suppressing noise during the switching of a differential circuit having differential inputs and outputs (col. 9, line 22- col. 10, line 66), comprising clocking the differential circuit after a transition of the signal at the differential output, the circulation of the charge being initiated by clocking the differential circuit, the resistor and capacitor having a time constant that is less than half the clocking frequency (col. 7, line 28- col. 8, line 67).

Regarding claims 20-22, Hilbert discloses an integrated circuit (fig. 4 and fig. 8), comprising: a differential circuit having a power input (col. 6, lines 10-65); the differential circuit further comprises a power return (col. 7, line 28- col. 8, line 67; col. 11, line 21- col. 12, line 13).

However, Hilbert does not specifically disclose an inductor having a first end coupled to the power input and a second end to couple to a power source; and a second inductor having a first end coupled to the power return and a second end to couple to a power source return.

On the other hand, Gardenfors et al, from the same field of endeavor, discloses a radio transceiver that can be completely integrated into one IC chip. A single, directly modulated VCO is used for both up-conversion during transmission, and down-conversion during reception.

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Furthermore, Gardenfors shows in figure 5, a transceiver on a chip, which includes a transmit/receive antenna coupled to a low noise amplifier in the receiver front end. The output of the low noise amplifier is coupled to an image-rejection mixer, which is also composed of a first mixer 206 for the I channel, a second mixer 208 for the Q channel, several phase shifters, and combiner (figs. 3-4; col. 5, line 41- col. 6, line 47). The transceiver on a chip also includes a phase locked loop, which is composed of a phase detector, a loop filter, and a prescaler with modulus logic 240. The phase locked loop is a component of a synthesizer, a charge pump, and a modulus logic circuitry 238 (fig. 5; col. 6, lines 48-67; col. 7, lines 1-44). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Gardenfors to the system of Hilbert in order to produce a short-range radio transceiver on a single integrated circuit chip.

Regarding claims 23-26, Hilbert discloses a circuit (fig. 8), comprising: a differential circuit; and a current source (807, 808, 813 of fig. 8) having an output coupled to the differential circuit; and the current source comprises a transistor (801- 804 of fig. 8) having a drain coupled to the differential circuit, a gate and a source, the capacitor being coupled between the gate and the source (col. 11, line 21- col. 12, line 62; col. 13, line 39- col. 14, line 60).

However, Hilbert does not specifically disclose a current source having an output coupled to the differential circuit, an input, and a capacitor shunting the input.

On the other hand, Gardenfors et al, from the same field of endeavor, discloses a radio transceiver that can be completely integrated into one IC chip. A single, directly modulated VCO is used for both up-conversion during transmission, and down-conversion during reception.

Furthermore, Gardenfors shows in figure 5, a transceiver on a chip, which includes a

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transmit/receive antenna coupled to a low noise amplifier in the receiver front end. The output of the low noise amplifier is coupled to an image-rejection mixer, which is also composed of a first mixer 206 for the I channel, a second mixer 208 for the Q channel, several phase shifters, and combiner (figs. 3-4; col. 5, line 41- col. 6, line 47). The transceiver on a chip also includes a phase locked loop, which is composed of a phase detector, a loop filter, and a prescaler with modulus logic 240. The phase locked loop is a component of a synthesizer, a charge pump, and a modulus logic circuitry 238 (fig. 5; col. 6, lines 48-67; col. 7, lines 1-44). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Gardenfors to the system of Hilbert in order to produce a short-range radio transceiver on a single integrated circuit chip.

Response to Arguments

3. Applicant's arguments filed on April 28, 2004 have been fully considered but they are not persuasive.

Applicant's representative argues that Hilbert cannot be properly combined with Gardenfors. In response to applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). References are evaluated by what they suggest to one versed in the art, rather than by their

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specific disclosure. In re Bozec, 163 USPQ 545 (CCPA) 1969. In this case, it would have been obvious for a person having ordinary skill in the pertinent art, at the time the invention was made, to apply the technique of Gardenfors to the system of Hilbert in order to produce a short-range radio transceiver on a single integrated circuit chip.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marceau Milord whose telephone number is 703-306-3023. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian C. Chin can be reached on 703-308-6739. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


MARCEAU MILORD

Marceau Milord
Examiner
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